

Appl. No. 10/074,881  
Amdt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

- 1        1. (Currently Amended) A method for monitoring electron charge effect
- 2        occurring during semiconductor processing, comprising the steps of:
- 3            providing a substrate, a layer of n-type conductivity having been created in said
- 4        substrate;
- 5            creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said
- 6        substrate, said pattern of LOCOS being interspersed with exposed regions of said
- 7        substrate;
- 8            etching said exposed regions of said substrate using said pattern of LOCOS
- 9        regions as a hard mask, creating a pattern of elevated LOCOS regions, creating
- 10      trenches having inside surfaces in said substrate;
- 11        creating a layer of interlayer oxide over said pattern of LOCOS regions and said
- 12      inside surfaces of said trenches created in said substrate;
- 13        depositing a layer of polysilicon over said layer of interlayer oxide;
- 14        patterning said layer of polysilicon, said patterned layer of polysilicon comprising
- 15      at least one contact point over said substrate, completing creation of a electron charge
- 16      monitoring device having a surface;
- 17        providing a semiconductor processing tool, said semiconductor processing tool
- 18      being designated as being a tool being evaluated for electron charge effect of a process
- 19      being performed by said tool;

Appl. No. 10/074,881  
Amdt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

20 positioning said substrate comprising said electron charge monitoring device  
21 inside said processing tool in a location and a position ~~being identical with a position~~  
22 and location being occupied by a substrate being processed by said tool;  
23 establishing processing conditions of a process as these processing conditions  
24 apply for said process and said tool;  
25 exposing said electron charge monitoring device to said established processing  
26 conditions for a period of time ~~having a measurable duration~~;  
27 terminating said processing conditions;  
28 removing said electron charge monitoring device from said semiconductor  
29 processing tool; and  
30 measuring a voltage required to induce a FN tunneling based current between  
31 the at least one contact point of said patterned layer of polysilicon and said substrate.  
1 2. (previously presented) The method of claim 1, said creating a pattern of  
2 Local Oxidation of Silicon (LOCOS) regions in said substrate comprising the steps of:  
3 depositing a layer of silicon nitride over said substrate;  
4 patterning said layer of silicon nitride, creating a mask of silicon nitride over said  
5 substrate, elements of said mask being interspersed with exposed regions of said  
6 substrate;  
7 creating layers of Local Oxidation of Silicon (LOCOS) in said exposed regions of  
8 said substrate; and  
9 removing said mask of silicon nitride from said substrate.

Appl. No. 10/074,881  
Amdt. dated 04/26/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: E0523-00004

- 1       3. (previously presented) The method of claim 1, wherein said layer of  
2 interlayer oxide is HTO, dry oxide or wet oxide.
- 1       4. (original) The method of claim 1, said layer of interlayer oxide being  
2 created to a thickness between about 80 and 300 Angstrom.
- 1       5. (currently amended) The method of claim 1, said layer of polysilicon being  
2 deposited to a thickness within the range of between about 1,500 and 6,000 Angstrom.
- 1       6. (currently amended) ~~The method as in claim 1, A method for monitoring~~  
2 electron charge effect occurring during semiconductor processing, comprising:  
3       providing a substrate, a layer of n-type conductivity having been created in said  
4       substrate;  
5       creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said  
6       substrate, said pattern of LOCOS being interspersed with exposed regions of said  
7       substrate;  
8       etching said exposed regions of said substrate using said pattern of LOCOS  
9       regions as a hard mask, creating a pattern of elevated LOCOS regions, creating  
10      trenches having inside surfaces in said substrate;  
11      creating a layer of interlayer oxide over said pattern of LOCOS regions and said  
12      inside surfaces of said trenches created in said substrate;  
13      depositing a layer of polysilicon over said layer of interlayer oxide;  
14      patterning said layer of polysilicon, said patterned layer of polysilicon comprising  
15      at least one contact point over said substrate, completing creation of a electron charge  
16      monitoring device having a surface;

Appl. No. 10/074,881  
Amdt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

17       providing a semiconductor processing tool, said semiconductor processing tool  
18       being designated as being a tool being evaluated for electron charge effect of a process  
19       being performed by said tool;  
20       positioning said substrate comprising said electron charge monitoring device  
21       inside said processing tool in a location and a position being occupied by a substrate  
22       being processed by said tool;  
23       establishing processing conditions of a process as these processing conditions  
24       apply for said process and said tool;  
25       exposing said electron charge monitoring device to said established processing  
26       conditions for a period of time;  
27       terminating said processing conditions;  
28       removing said electron charge monitoring device from said semiconductor  
29       processing tool; and  
30       measuring a voltage required to induce a FN tunneling based current between  
31       the at least one contact point of said patterned layer of polysilicon and said substrate,  
32        said patterned layer of polysilicon comprising a square, said pattern of Local  
33       Oxidation of Silicon (LOCOS) regions comprising arrays of LOCOS regions  
34       perpendicularly and outwardly extending from each side of said square of said  
35       patterned layer of polysilicon.

1       Claims 7-11: (cancelled)

1       12. (currently amended) The method of claim 1, said current induced between  
2       said layer of polysilicon and said substrate being about 0.1  $\mu$ A.

Appl. No. 10/074,881  
Amdt. dated 04/26/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: E0523-00004

- 1        13. (currently amended) A method of creating an electron charge effect
- 2        monitoring device, comprising ~~the steps of~~:
- 3                providing a substrate, a layer of n-type conductivity having been created in said
- 4        substrate;
- 5                creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said
- 6        substrate, said pattern of LOCOS being interspersed with exposed regions of said
- 7        substrate;
- 8                etching said exposed regions of said substrate using said pattern of LOCOS
- 9        regions as a hard mask, creating a pattern of elevated LOCOS regions, creating
- 10      trenches having inside surfaces in said substrate;
- 11                creating a layer of interlayer oxide over said pattern of LOCOS regions and said
- 12      inside surfaces of said trenches created in said substrate;
- 13                depositing a layer of polysilicon over said layer of interlayer oxide;
- 14                patterning said layer of polysilicon, said patterned layer of polysilicon comprising
- 15      at least one contact point over said substrate; and
- 16                measuring a voltage required to induce a FN tunneling based current between
- 17      said at least one contact point of said patterned layer of polysilicon and said substrate
- 18      after said substrate has been exposed to a semiconductor processing tool under known
- 19      conditions of processing by said semiconductor processing tool.
- 1        14. (previously presented) The method of claim 13, said creating a pattern of
- 2        Local Oxidation of Silicon (LOCOS) regions in said substrate comprising ~~the steps of~~:
- 3                depositing a layer of silicon nitride over said substrate;

Appl. No. 10/074,881  
Amdt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

4 patterning said layer of silicon nitride, creating a mask of silicon nitride over said  
5 substrate, elements of said mask being interspersed with exposed regions of said  
6 substrate;

7 creating layers of Local Oxidation of Silicon (LOCOS) in said exposed regions of  
8 said substrate; and

9 removing said mask of silicon nitride from said substrate.

1 15. (previously presented) The method of claim 13, wherein said layer of  
2 interlayer oxide is HTO, dry oxide or wet oxide.

1 16. (original) The method of claim 13, said layer of interlayer oxide being  
2 created to a thickness between about 80 and 300 Angstrom.

1 17. (currently amended) The method of claim 13, said layer of polysilicon  
2 being deposited to a thickness within the range of between about 1,500 and 6,000  
3 Angstrom.

1 18. (currently amended) The method of claim 13, A method of creating an  
2 electron charge effect monitoring device, comprising:

3 providing a substrate, a layer of n-type conductivity having been created in said  
4 substrate;

5 creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said  
6 substrate, said pattern of LOCOS being interspersed with exposed regions of said  
7 substrate;

Appl. No. 10/074,881  
Amdt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

8       etching said exposed regions of said substrate using said pattern of LOCOS  
9       regions as a hard mask, creating a pattern of elevated LOCOS regions, creating  
10      trenches having inside surfaces in said substrate;  
11      creating a layer of interlayer oxide over said pattern of LOCOS regions and said  
12      inside surfaces of said trenches created in said substrate;  
13      depositing a layer of polysilicon over said layer of interlayer oxide;  
14       patterning said layer of polysilicon, said patterned layer of polysilicon comprising  
15      at least one contact point over said substrate; and  
16      measuring a voltage required to induce a FN tunneling based current between  
17      said at least one contact point of said patterned layer of polysilicon and said substrate  
18      after said substrate has been exposed to a semiconductor processing tool under known  
19      conditions of processing by said semiconductor processing tool,  
20        said patterned layer of polysilicon comprising a square, said pattern of Local  
21      Oxidation of Silicon (LOCOS) regions comprising arrays of LOCOS regions  
22      perpendicularly and outwardly extending from each side of said square of said  
23      patterned layer of polysilicon.

1       Claims 19-22: (cancelled).

1       23. (previously presented) The method of claim 13, whereby said electron  
2      charge effect monitoring device can be recycled by applying an additional step of  
3      thermally annealing said substrate, thereby thermally annealing said electron charge  
4      monitoring device having been created in and on said substrate.

1       Claims 24-32 (cancelled).

Appl. No. 10/074,881  
Amdt. dated 04/26/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: E0523-00004

- 1        33. (newly added)      A method for monitoring electron charge effect
- 2        occurring during semiconductor processing, comprising:
  - 3           forming a monitor wafer having floating gate structures;
  - 4           exposing the monitor wafer to a plasma process; and
  - 5           measuring plasma damage by measuring interlayer oxide electron trap out rate.
- 1        34. (newly added)      The method of claim 33, said measuring interlayer oxide electron trap out rate comprising measuring a voltage required to induce a FN tunneling based current between at least one contact point of said floating gate structures and said monitor wafer.
- 1        35. (newly added)      The method of claim 34, said FN tunneling based current between at least one contact point of said floating gate structures and said monitor wafer being about 0.1  $\mu$ A.
- 1        36. (newly added)      A method for monitoring electron charge effect
- 2        occurring during semiconductor processing, comprising:
  - 3           providing a monitor substrate having a layer of n-type conductivity therein and
  - 4           including oxidized regions formed thereover and interspersed with trench regions that
  - 5           each include an opening extending into said monitor substrate, an interlayer oxide layer disposed over said oxidized regions and said trench regions, a patterned polysilicon
  - 7           layer disposed over said interlayer oxide layer and comprising at least one contact point
  - 8           over said monitor substrate that forms an electron charge monitoring device having a
  - 9           surface;

Appl. No. 10/074,881  
Arndt. dated 08/24/04  
Reply to Office Action of 02/24/2004

Attorney Docket No.: N1085-90059

- 10 providing a semiconductor processing tool designated as being evaluated for
- 11 electron charge effect of a process being performed by said semiconductor processing
- 12 tool;
- 13 positioning said monitor substrate inside said semiconductor processing tool in a
- 14 location and a position generally occupied by a substrate being processed by said
- 15 semiconductor processing tool;
- 16 establishing processing conditions for said process;
- 17 exposing said electron charge monitoring device to said established processing
- 18 conditions for a period of time;
- 19 removing said electron charge monitoring device from said semiconductor
- 20 processing tool; and
- 21 measuring a voltage required to induce a FN tunneling based current between
- 22 the at least one contact point of said patterned layer of polysilicon and said monitor
- 23 substrate.